IN THE CLAIMS:

Please note that all claims in the referenced application are shown below. New claims 98-108 have been added.

Please cancel claims 36-75 and 87-97 without prejudice or disclaimer to the filing of a divisional application.

Please enter the claims as amended.

1. (Twice Amended) A stacked semiconductor assembly, comprising:

a first semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads electrically connected to integrated circuitry of said first semiconductor die, said at least one redistribution bond pad circuit ~~independent~~ electrically isolated from said integrated circuitry of said first semiconductor die and including a plurality of redistribution bond pads;

a second semiconductor die including an active surface, a backside, and a plurality of bond pads on said active surface thereof, said active surface of said second semiconductor die facing said active surface of said first semiconductor die; and

at least one electrical connector extending between at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die and at least one redistribution bond pad of said plurality of redistribution bond pads on said first semiconductor die.

2. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein said first semiconductor die is disposed on a substrate.

3. (Previously Amended) The stacked semiconductor assembly of claim 2, wherein said first semiconductor die is electrically connected to said substrate with intermediate conductive elements.

4. (Previously Amended) The stacked semiconductor assembly of claim 3, wherein said intermediate conductive elements comprise bond wires.

5. (Previously Amended) The stacked semiconductor assembly of claim 2, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said first semiconductor die.

6. (Previously Amended) The stacked semiconductor assembly of claim 5, wherein said second redistribution bond pad is electrically connected to said substrate.

7. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein peripheral edges of said first semiconductor die and edges of said second semiconductor die are substantially vertically aligned.

8. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein said second semiconductor die is smaller than said first semiconductor die.

9. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector spaces the active surface of said second semiconductor die from the active surface of said first semiconductor die.

10. (Previously Amended) The stacked semiconductor assembly of claim 1, further comprising a substrate under said first semiconductor die, said substrate including a plurality of contact areas thereon.

11. (Previously Amended) The stacked semiconductor assembly of claim 10, wherein at least one bond pad of said plurality of bond pads on said first semiconductor die is electrically connected to a corresponding contact area of said plurality of contact areas on said substrate.

12. (Previously Amended) The stacked semiconductor assembly of claim 10, wherein said at least one redistribution bond pad is electrically connected to a corresponding contact area of said plurality of contact areas on said substrate.

13. (Twice Amended) The stacked semiconductor assembly of claim 10, further comprising at least one semiconductor die vertically stacked on said substrate, wherein said backside of said first semiconductor die is located above said at least one stacked semiconductor die.

14. (Previously Amended) The stacked semiconductor assembly of claim 1, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

15. (Previously Amended) The stacked semiconductor assembly of claim 14, wherein said insulative layer comprises an adhesive material.

16. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector comprises a substantially columnar pillar.

17. (Previously Amended) The stacked semiconductor assembly of claim 16, wherein said substantially columnar pillar is copper.

18. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein said at least one electrical connector comprises a solder ball.

19. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein at least one peripheral edge of said second semiconductor die extends laterally beyond at least one corresponding peripheral edge of said first semiconductor die.

20. (Previously Amended) The stacked semiconductor assembly of claim 19, further comprising at least one electrical connector extending from at least one bond pad of said plurality of bond pads on said second semiconductor die and a corresponding contact area of a substrate.

21. (Previously Amended) The stacked semiconductor assembly of claim 1, wherein at least one peripheral edge of said first semiconductor die extends laterally beyond at least one corresponding peripheral edge of said second semiconductor die.

22. (Twice Amended) A semiconductor assembly, comprising:

a substrate;

a first semiconductor die including an active surface, a second surface, and a plurality of peripheral edges, said second surface disposed on said substrate, said active surface having a plurality of bond pads thereon;

a second semiconductor die including an active surface, a second surface, a plurality of peripheral edges and a plurality of bond pads on said active surface, said active surface of said second semiconductor die facing said active surface of said first semiconductor die, <u>at least one bond pad of said plurality of bond pads of said first semiconductor die communicating with a corresponding redistribution circuit of said second semiconductor die, said redistribution circuit being electrically isolated from integrated circuitry of said second semiconductor die,</u> at least one edge of said plurality of peripheral edges of said second semiconductor die extending laterally beyond at least one corresponding peripheral edge of said plurality of peripheral edges of said first semiconductor die; and

at least one connective element extending from at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die to a corresponding contact

area of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die.

23. (Original) The semiconductor assembly of claim 22, further comprising at least one additional semiconductor die stacked vertically between said first semiconductor die and said second semiconductor die.

24. (Previously Amended) The semiconductor assembly of claim 23, wherein said at least one additional semiconductor die and said first semiconductor die are all electrically connected to said substrate by discrete conductive elements.

25. (Previously Amended) The semiconductor assembly of claim 23, wherein a third semiconductor die of said at least one additional semiconductor die is disposed directly below said second semiconductor die, said third semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads of said third semiconductor die electrically connected to integrated circuitry of said third semiconductor die, said at least one redistribution bond pad circuit independent from the integrated circuitry of said third semiconductor die and including a plurality of redistribution bond pads.

26. (Original) The semiconductor assembly of claim 25, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of redistribution bond pads, said second redistribution bond pad proximate the perimeter of said third semiconductor die.

27. (Previously Amended) The semiconductor assembly of claim 26, wherein at least one connective element extends between said least one bond pad on said active surface of said second semiconductor die and said first redistribution bond pad on said active surface of said third semiconductor die.

28. (Original) The semiconductor assembly of claim 27, wherein said second redistribution bond pad is electrically connected to said substrate by discrete conductive elements.

29. (Original) The semiconductor assembly of claim 24, wherein said discrete conductive elements comprise at least one of wire bonds, TAB elements, and leads.

30. (Previously Amended) The semiconductor assembly of claim 22, wherein said at least one connective element comprises a substantially columnar pillar.

31. (Original) The semiconductor assembly of claim 30, wherein said substantially columnar pillar is copper.

32. (Original) The semiconductor assembly of claim 22, wherein said at least one connective element comprises a solder ball.

33. (Original) The semiconductor assembly of claim 22, wherein said at least one connective element extends from said at least one bond pad of said second semiconductor die to said corresponding contact area of said substrate.

34. (Original) The semiconductor assembly of claim 22, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

36 through 75 (previously withdrawn and canceled without prejudice or disclaimer herein).

76. (Amended) A semiconductor device for use in a stacked semiconductor assembly, said semiconductor device comprising:

a backside;

an active surface including a plurality of bond pads; and

at least one redistribution bond pad circuit on said active surface, said at least one redistribution bond pad circuit ~~independent~~ electrically isolated from integrated circuitry of said semiconductor device.

77. (Previously Amended) The semiconductor device of claim 76, wherein said plurality of bond pads is electrically connected to said integrated circuitry of said semiconductor device.

78. (Previously Amended) The semiconductor device of claim 77, wherein said plurality of bond pads is centrally located on said active surface.

79. (Previously Amended) The semiconductor device of claim 77, wherein said plurality of bond pads is located proximate the perimeter of said active surface.

80. (Previously Amended) The semiconductor device of claim 76, wherein said at least one redistribution bond pad circuit comprises a first redistribution bond pad electrically connected to a second redistribution bond pad.

81. (Previously Amended) The semiconductor device of claim 80, wherein said at least one redistribution bond pad circuit further comprises a conductive trace extending between said first redistribution bond pad and said second redistribution bond pad.

81. (Previously Amended) The semiconductor device of claim 80, wherein said at least one redistribution bond pad circuit further comprises a conductive trace extending between said first redistribution bond pad and said second redistribution bond pad.

82. (Original) The semiconductor device of claim 81, wherein said conductive trace comprises at least one of titanium, copper, aluminum, NiV and nickel.

83. (Original) The semiconductor device of claim 80, wherein said first redistribution bond pad is located on said active surface in a location that mirrors a location of a corresponding bond pad of a second semiconductor device to be positioned above said semiconductor device.

84. (Original) The semiconductor device of claim 83, wherein said second redistribution bond pad is proximate the perimeter of said semiconductor device.

85. (Original) The semiconductor device of claim 80, wherein said first redistribution bond pad is electrically connected to a corresponding bond pad on an active surface of a second semiconductor device.

86. (Original) The semiconductor device of claim 85, wherein said second redistribution bond pad is electrically connected to a contact area on a substrate.

87 through 97 (previously withdrawn and canceled without prejudice or disclaimer herein).

Please add the following new claims:

98. (New) A semiconductor assembly, comprising:

a substrate;

a first semiconductor die including an active surface, a second surface, and a plurality of peripheral edges, said second surface disposed on said substrate, said active surface having a plurality of bond pads thereon;

a second semiconductor die including an active surface, a second surface, a plurality of peripheral edges and a plurality of bond pads on said active surface, said active surface of said second semiconductor die facing said active surface of said first semiconductor die, at least one edge of said plurality of peripheral edges of said second semiconductor die extending laterally beyond at least one corresponding peripheral edge of said plurality of peripheral edges of said first semiconductor die;

a third semiconductor die disposed directly below said second semiconductor die, said third semiconductor die including an active surface and a backside, said active surface including a plurality of bond pads and at least one redistribution bond pad circuit thereon, said plurality of bond pads of said third semiconductor die electrically connected to integrated circuitry of said third semiconductor die, said at least one redistribution bond pad circuit independent from the integrated circuitry of said third semiconductor die and including a plurality of redistribution bond pads; and

at least one connective element extending from at least one bond pad of said plurality of bond pads on said active surface of said second semiconductor die to a corresponding contact area of said substrate adjacent to said at least one corresponding peripheral edge of said first semiconductor die.

99. (New) The semiconductor assembly of claim 98, wherein said at least one redistribution bond pad circuit comprises a plurality of conductive traces, at least one conductive trace of said plurality of conductive traces connecting a first redistribution bond pad of said plurality of redistribution bond pads and a second redistribution bond pad of said plurality of

redistribution bond pads, said second redistribution bond pad proximate the perimeter of said third semiconductor die.

100. (New) The semiconductor assembly of claim 99, wherein at least one connective element extends between said least one bond pad on said active surface of said second semiconductor die and said first redistribution bond pad on said active surface of said third semiconductor die.

101. (New) The semiconductor assembly of claim 100, wherein said second redistribution bond pad is electrically connected to said substrate by discrete conductive elements.

102. (New) The semiconductor assembly of claim 98, wherein said discrete conductive elements comprise at least one of wire bonds, TAB elements, and leads.

103. (New) The semiconductor assembly of claim 98, wherein said at least one connective element comprises a substantially columnar pillar.

104. (New) The semiconductor assembly of claim 103, wherein said substantially columnar pillar is copper.

105. (New) The semiconductor assembly of claim 98, wherein said at least one connective element comprises a solder ball.

106. (New) The semiconductor assembly of claim 98, wherein said at least one connective element extends from said at least one bond pad of said second semiconductor die to said corresponding contact area of said substrate.

107. (New) The semiconductor assembly of claim 98, further comprising an insulative layer between said first semiconductor die and said second semiconductor die.

108. (New) The semiconductor assembly of claim 107, wherein said insulative layer comprises an adhesive material.